WHAT IS CLAIMED IS:

1. A multilayer semiconductor device assembly jig, comprising:

a base member for serially layering a plurality of semiconductor modules each including a semiconductor chip mounted on a thin printed-wiring board and a bump on each of a plurality of interlayer connection lands;

a position restriction mechanism for layering said semiconductor modules on said base member with their positions mutually restricted;

a height restriction mechanism for restricting an entire height of said semiconductor module group layered on said base member;

an evenness holding mechanism for maintaining evenness of a top-layer semiconductor module; and

an alignment mechanism for providing alignment with reference to a mother substrate where a layered semiconductor module unit is mounted,

wherein said assembly jig performs interlayer connection among said semiconductor modules by applying reflow heating to melt each of said bumps, is inverted to be positioned and combined with said mother substrate via said alignment mechanism, and is removed after the interlayer connection between this mother substrate and a first-layer semiconductor module of said layered semiconductor module unit.

2. The multilayer semiconductor device assembly jig according to claim 1 having a box-shaped member which is assembled on said base member and comprises a storage

space for storing the specified number of said semiconductor modules in a layered state,

wherein an inner wall of said storage space constitutes said position restriction mechanism by supporting an outer periphery of said semiconductor module.

3. The multilayer semiconductor device assembly jig according to claim 2, wherein said alignment mechanism comprises a plurality of positioning pins and positioning holes correspondingly formed on an opening end of said box-shaped member and said mother substrate.

4. The multilayer semiconductor device assembly jig according to claim 1, wherein said position restriction mechanism comprises a plurality of positioning pins provided on said base member and used for locking at least three different positions of an outer periphery of said semiconductor module.

5. The multilayer semiconductor device assembly jig according to claim 1, wherein said position restriction mechanism comprises a plurality of positioning pins provided on said base member for piercing through positioning holes formed in marginal regions of said semiconductor modules.

6. The multilayer semiconductor device assembly jig according to claim 5, wherein said positioning pin is also used for said alignment mechanism with a tip thereof piercing through a positioning hole formed on said mother substrate.

7. The multilayer semiconductor device assembly jig according to claim 1, wherein said height restriction mechanism comprising:

a box-shaped member assembled on said base member and provided with a storage space therein for storing the specified number of said semiconductor modules in a layered state; and

a cover member assembled to said box-shaped member by pressing a top-layer semiconductor module placed in said storage space.

8. A multilayer semiconductor device manufacturing method using an assembly jig for mutually restricting positions of a plurality of semiconductor modules each including a semiconductor chip mounted on a thin printed-wiring board and a bump on each of a plurality of interlayer connection lands through the use of a position restriction mechanism, layering said modules with an entire height restricted through the use of a height restriction mechanism, and maintaining evenness of a top-layer semiconductor module through the use of a evenness holding mechanism, comprising the steps of:

serially layering the specified number of said semiconductor modules on said base member with respective positions restricted by said position restriction mechanism and placing layered modules in said assembly jig with an entire height restricted by said height restriction mechanism;

supplying said assembly jig into a reflow furnace, applying reflow heating to melt said each bump for interlayer connection among said semiconductor modules, and forming a layered semiconductor module unit; and

mounting said layered semiconductor module unit on a mother substrate by

using a top-layer semiconductor module as a junction module with evenness maintained by said evenness holding mechanism.

9. The multilayer semiconductor device manufacturing method according to claim 8, providing said assembly jig with an alignment mechanism for aligning said layered semiconductor module unit against said mother substrate for mounting, comprising the steps of:

positioning and combining said assembly jig, inverted after forming layered semiconductor module unit, with said mother substrate via said alignment mechanism;

supplying an assembly of said assembly jig and said mother substrate into a reflow furnace and applying reflow heating for interlayer connection between a first-layer semiconductor module in said layered semiconductor module unit and said mother substrate; and

removing said assembly jig from said mother substrate.

10. The multilayer semiconductor device manufacturing method according to claim 8 using said printed-wiring board having interlayer connection lands and dummy lands corresponding to interlayer connection lands on all printed-wiring boards for respective layers, comprising the step of:

forming a bump on each of connection lands and dummy lands of said printed-wiring board for each semiconductor module.